Abstract— This paper presents a layout design methodology for monolithic microwave integrated circuits, which leads to the optimized layout in a fast and efficient way, avoiding time-consuming computer simulations. The proposed procedure is based on subdividing the layout in simple basic cells that are individually optimized. Optimization of each layout basic cell is performed to compensate for parasitic effects associated to circuit components as well as for the effect of short length transmission lines that are added to layout as interconnections. This procedure points out which components are more troublesome to be manufactured and helps the designer to choose a circuit topology that leads to high fabrication yield. As an application example, the layout design of a 5 to 10 GHz LC band-pass filter is presented.

Index Terms— Layout, MMIC, monolithic microwave integrated circuits.

I. INTRODUCTION

The layout of microwave circuits is always a challenge to the designer and becomes especially critical in case of MMICs where you are not allowed to trim the circuit after fabrication. Passive and active components of the circuit tend to deviate from their ideal models as operation frequency enters the Gigahertz band. Also, metallic interconnections between components behave as reactances, modifying designed circuit performance. Reactive parasitic effects and losses of the real elements affect frequency response characteristics of the circuit, as bandwidth, gain or insertion loss.

The microwave circuit designer cannot eliminate parasitic effects associated to components and metallic interconnections used in the circuit, but it is possible to obtain a more realistic evaluation of the prototype performance through post layout simulations, employing models that represent the behavior of components and metallic interconnections at microwave frequencies. If circuit specifications are not reached, layout alterations and circuit simulations can be iteratively applied, aiming at optimizing circuit performance. Although that procedure can lead to good results, it is very time-consuming, especially when circuit is complex. Moreover the designer cannot be sure the best possible performance for the designed circuit was achieved.

This paper proposes a step-by-step layout design methodology for microwave monolithic integrated circuits that conducts to the optimized layout design in a simple and efficient way. The result is a circuit whose performance is as close as possible to specifications, considering circuit topology and

Methodology for MMIC Layout Design

Fatima Salete Correra¹ and Eduardo Amato Tolezani²,
¹Laboratório de Microeletrônica da USP, Av. Prof. Luciano Gualberto, tr. 3, n.158, CEP 05508-970, São Paulo, SP, Brazil, fcorrera@lme.usp.br
²Ominisys Engenharia Ltda., R. Lourdes, 560, CEP 09571-470, São Caetano do Sul, SP, Brazil, tolezani@omnisys.com.br
fabrication technology used. That procedure also evidences which components are more critical for manufacturing, so that it can guide the designer to perform changes in the topology, or in the circuit, to increase its robustness.

The following sections describe the proposed layout design methodology and its application to the layout design of a band-pass LC filter in MMIC technology.

II. LAYOUT DESIGN METHODOLOGY

The layout design methodology is represented in flow chart of Figure 1. The information required for layout development are: circuit schematic; layout rules for the chosen circuit construction technology; criteria to avoid undesirable electromagnetic coupling; and a library containing layout artwork and models to represent circuit components response in the frequency band of interest [1].

![Flow chart of the layout design methodology.](image)

A. Pre-layout

The first step is to define a preliminary layout, by replacing designed circuit components with the respective available foundry layout artworks.

This pre-layout must consider foundry layout rules for the MMIC technology chosen in order to guarantee high production yielding. In addition, the designer should simultaneously minimize circuit area and undesirable electromagnetic coupling among components that could degrade prototype’s performance.

Layout rules are supplied by the foundry that set minimum dimensions and distances among...
dielectric, resistive and conductive layers used in MMIC construction. These dimensions and distances are in the order of some microns and do not constitute significant limitations to the layout.

However, avoiding undesirable electromagnetic coupling inside the circuit is more critical. Planar inductors, transmission lines or other structures with length greater than $\lambda/10$ in the operation frequency band are sensitive to electromagnetic coupling in ways that are not usually accounted for in circuit simulation software.

In order to minimize undesirable electromagnetic coupling, the designer must consider two parameters: distance and relative positioning among all circuit components in the pre-layout. It is recommended to keep electromagnetic coupling sensitive components away from via-holes, other components and substrate edges. A criterion usually applied is to use a minimum distance of 1.5 times the height of the substrate between them [2].

In addition, the layout designer should avoid placing side-by-side structures that are sensitive to electromagnetic coupling. Figure 2 illustrates how the relative position of two inductors can be optimized in order to reduce electromagnetic coupling between them and as a result, the risk of undesirable circuit oscillations.

Preliminary layout is completed by adding metallic strips to interconnect circuit components. These metallic interconnections behave as short transmission lines. The effect of these additional elements on circuit performance should be compensated afterwards.

B. Splitting of layout in Basic cells

The next step is to split pre-layout in basic cells that will be optimized individually. These basic cells should not be too complex to avoid very time-consuming simulation, leading to efficient computer optimization.

A basic cell can be composed by single components – R, L or C, or by components in series or shunt associations – LC, RC, RL or RLC. In addition, the basic cell should contain transmission lines and via-holes associated to circuit pre-layout components, so that their effect could be considered during the optimization step.
Proposed criteria for definition of the layout basic cells are:

- Simple basic cells, containing only one passive circuit component: these cells are used to optimize isolated circuit components together with pre-layout associated transmission lines and via-holes. Figure 3 shows the layout basic cell associated to an ideal inductor.

- Composed basic cells, containing more than one passive circuit component: these cells are used to optimize series or shunt associated components layout – LC, RC, RL or RLC. In addition, these cells should contain transmission lines and via-holes associated to the components in circuit pre-layout, so that their effect can be considered during the composed basic cell optimization. Figure 4 illustrates the basic cell of a series connected LC association.

- Active basic cells, containing a transistor and components used to stabilize it: these cells are used to optimize the block composed by a transistor and components associated for stabilization purposes, as well as transmission lines and via-holes required for interconnections. Layout of these cells is critical and needs to be carefully optimized as to avoid potential instability of the transistor without excessive degradation of gain, noise or any other relevant parameter. Figure 5 illustrates the basic cell of a HEMT transistor associated to an RC stabilization circuit.

![Fig. 3. Ideal inductor and respective layout cell.](image)

![Fig. 4. Ideal series LC circuit and its respective layout cell.](image)
C. Optimization of layout basic cells

Every layout basic cell is individually optimized by comparing its electrical performance in the frequency band of interest to the response of the circuit component or components that it replaces. Layout basic cell optimization is performed by slightly changing physical dimensions of its elements, such as number of turns and line width of planar inductors and area of MIM capacitors. Dimensions of transmission lines used to interconnect layout components can act as additional optimization parameters. If needed, the length of these transmission lines can be increased and its width adjusted during layout cells optimization.

Comparison between an ideal component or components association and its layout cell at microwave frequencies can be performed using their scattering parameters referenced to system impedance $Z_0$.

Larger accuracy can be obtained using generalized scattering parameters [3]. In this case, the impedances at the component ports when it is immersed in the circuit are used as reference impedances for calculation of the $S$ matrix instead of $Z_0$. That procedure allows a more precise visualization on how layout basic cell performance will affect circuit response.

D. Integration of layout basic cells

Once all basic cells were individually optimized, they are interconnected to integrate the layout of the designed circuit, which is expected to be close to the optimum layout, for the circuit topology adopted.

The layout is then used to generate the complete schematic to be used in post-layout simulations. In this schematic, passive and active components are represented by electrical equivalent circuit models or by black box models, as $S$ parameter data files. Metallic strips used to interconnect the circuit components are modeled as transmission lines. The complete schematic should additionally include models to account for the effect of T, PI or other junctions used in the layout.
E. Post-layout simulation and final optimization

Post-layout simulation is performed using the complete circuit schematic and comparing its electrical performance to the ideal circuit response.

Considering that each layout cell was individually optimized, the post-layout simulation results should be close to the circuit specifications with regard to functionality and frequency response characteristics. A slightly improvement on circuit performance can be obtained by a final optimization of the layout.

Losses associated to layout components will affect the module of circuit return and transmission losses. In case that the effect of losses is incompatible with circuit specifications, the designer should consider other circuit topologies, or the choice of other technology for circuit implementation.

III. APPLICATION EXAMPLE – 5 TO 10 GHz BAND-PASS FILTER

As an example, it will be considered a 5 to 10 GHz LC band-pass filter, whose schematic is presented in Figure 6. The filter was designed using exact synthesis [4]. It is composed by ideal lumped inductors and capacitors. The exact synthesis software proposed a set of filter topologies that met the input specifications. Topologies with components values out of the range recommended by the foundry were discarded. The filter topology presented in Figure 6 was selected because it presented the smallest sensitivity to variations on component values. Filter response is presented in Figure 7.

Fig. 6. 5 to 10 GHz LC band-pass filter schematic.
Assuming the circuit would be built using MMIC technology with 100 μm thick substrate, the filter pre-layout shown in Figure 8 was designed as follows:

- Ideal inductors and capacitors were replaced with planar inductors and MIM capacitors available in the foundry library, with the same nominal values as the corresponding ideal components;
- connections to ground were accomplished by via-holes in pre-layout;
- inductors were placed alternately in pre-layout, so as to minimize electromagnetic coupling among them;
- the length of metallic strips used to interconnect circuit components were set so that RF sensitive elements were at least 150 μm apart from each other, and also from transmission lines, via-holes and layout edges;
- input and output pads for RF signals were added, connected by means of 50 Ω transmission lines.

A strong degradation on filter performance can be observed after performing simulation of the pre-layout electric equivalent circuit. Figure 9 compares the ideal filter frequency response and the pre-layout equivalent circuit frequency response. Pre-layout simulation showed worst results for filter loss and impedance matching when compared to the ideal filter. Additionally, the pass-band of the filter was narrowed and shifted towards lower frequencies, due to layout parasitic effects.
The pre-layout was split into 5 basic cells, as illustrated in Figure 10, where LC parallel resonators are highlighted in yellow, LC series resonators in green and input and output RF pads are detached in orange.

![Fig. 10. Basic cells of the band-pass filter layout.](image)

Layout basic cells were individually tuned, in order to fit their performances to that of their corresponding ideal resonators. Amplitude and phase of the S-parameters were compared. Due to symmetry of the filter circuit, cells A and E are identical and so are cells B and D. Figure 11 presents one of the filter LC parallel resonators and its respective layout basic cell, Values shown were obtained after optimization.

Dimensions of the spiral planar inductor and the MIM capacitor were optimized in order to minimize return loss phase error between the ideal resonator and its layout basic cell.

Notice that the optimized planar inductor value – 0.664 nH, is smaller than the ideal one– 0.693 nH, to compensate for the inductive effect of series microstrip transmission lines. Capacitance of MIM capacitor was reduced from its initial value – 0.73 pF, to 0.52 pF, accounting for the contribution of planar inductor parasitic capacitance to ground.

Figure 12 shows return loss vs. frequency curves obtained for the ideal LC resonant circuit and its optimized layout cell. One notices an excellent phase agreement of both curves from 100 MHz to 15 GHz. Magnitude error observed in Figure 12 is mainly due to resistive losses of real planar inductor.
The optimized layout basic cells were integrated to generate the filter layout and a post-layout simulation was performed, without any additional optimization. Figure 13 presents the post-layout simulation results compared to the ideal filter frequency response.

The procedure of individually optimizing each layout basic cell led to recover filter bandwidth. Lower and upper cut-off frequencies obtained on filter post-layout simulation are very close to the values obtained with the ideal circuit. A great improvement was observed on filter return loss compared to pre-layout simulation results presented at Figure 9. However, filter insertion loss was increased when compared to the ideal filter, mainly due to resistive losses of planar inductors used in the filter. Additional improvement on the insertion loss would demand for the search of other filter topologies or technologies with lower losses.
A Monte Carlo yield analysis was performed in order to estimate manufacturing yield of the designed filter. Table I presents the standard deviations used on Monte Carlo analysis for passive components.

<table>
<thead>
<tr>
<th>Category</th>
<th>Circuit parameters</th>
<th>Standard deviation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmission lines</td>
<td>Plated line width</td>
<td>0.5 μm</td>
</tr>
<tr>
<td>Capacitors</td>
<td>Capacitance</td>
<td>3.3 %</td>
</tr>
<tr>
<td>Inductors</td>
<td>Plated line width</td>
<td>0.5 μm</td>
</tr>
<tr>
<td>Substrate</td>
<td>Thickness</td>
<td>2.8 μm</td>
</tr>
</tbody>
</table>

The Monte Carlo analysis of the filter was performed with 300 trials, and its results are presented in Figure 14.

The methodology here proposed was also successfully applied to the layout design of a 5 to 10 GHz two-stage PHEMT amplifier, designed using direct synthesis, demonstrating its feasibility for higher complexity circuits [5].
IV. CONCLUSIONS

A step-by-step methodology for MMIC layout design was proposed, that consists in splitting the layout in basic cells, which are optimized individually.

That procedure results in high computational efficiency due to low complexity of layout basic cells. In addition, the designer can identify critical circuit components that are difficult to be implemented using the construction technology adopted. Thus, the designer can fine-tune the designed circuit aiming at increasing its feasibility and robustness.

Although it is not possible to obtain the exact frequency response of an ideal circuit, the layout design methodology proposed here leads to optimized solutions, resulting in a good approach to the ideal circuit, with performance limitations imposed by characteristics of the adopted MMIC technology.

ACKNOWLEDGMENTS

The authors thank Dr. Denise Consonni for helpful suggestions on manuscript preparation and CAPES for the financial support to this work.

REFERENCES